Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **C**
4. **N.G2A**
5. **N.G2B**
6. **G1**
7. **Y7**
8. **GND**
9. **Y6**
10. **Y5**
11. **Y4**
12. **Y3**
13. **Y2**
14. **Y1**
15. **Y0**
16. **VCC**

**.056”**

**.067”**

**14**

**13**

**12**

**11**

**2 1 16 15**

**7 8 9 10**

**3**

**4**

**5**

**6**

**HCT**

**138G**

**MASK**

**REF**

**NOTE: PAD #16 TO BE BONDED FIRST**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC (or leave FLOATING)**

**Mask Ref: HCT138G**

**APPROVED BY: DK DIE SIZE .056” X .067” DATE: 8/30/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HCT138**

**DG 10.1.2**

#### Rev B, 7/19/02